Project 3.2:

(a) **Title:** Effect of Temperature and Electric Field on Polysilicon Gettering of Copper Impurities in Silicon Wafers

(b) **Objective:** To investigate the effects of temperature and an external electric field on polysilicon gettering of copper impurities in different types of silicon wafers

(c) **Type of Research:** Process & Technology Development

(d) **Beneficiaries of the Project:** Electronics industry

(e) **Products/Services:** M.Eng thesis

(f) **Researchers:** Choong Chwee Lin, Dr W. P. Lee, Assoc. Prof H.K. Yow, and Prof T.Y. Tou

(g) **Status of Progress:** Work completed. The student thesis (M.Eng) submitted in April 2006

(h) **Targeted Date of Completion:** April 2006

(i) **Source of Funding:** Funded by S.E.H. (M) Sdn Bhd. and Motorola Foundation Grant.

(j) **Abstract:**

Polysilicon film is a simple medium commonly used in gettering technique to reduce copper impurities level in silicon wafer bulk. However, polysilicon gettering using polysilicon deposited at the wafer back surface could not segregate the copper in the wafer bulk below the limitation level of $2 \times 10^9 \text{cm}^2$ after device processing in the VLSI/ULSI technology. In this work, a parametric study was carried out on copper impurities to investigate the limitations of polysilicon gettering, with respect to different types of substrate. These factors include the annealing temperature and duration, dopant type and doping level in the substrate, and also the application of electric field to produce a directional drift of positively charged copper ions towards the gettering sink. The experimental results correlate well with the behavior of copper in silicon, where the segregation coefficient is strongly dependent on copper solubility and diffusivity, which are also a function of both temperature and acceptor doping level of sample due to the positively charged state of copper interstitials. A significant outcome of this work is an optimized polysilicon gettering technique incorporating annealing at moderate temperature of $760^\circ \text{C}$, followed by negative biasing at $-11 \text{kV/cm}$ in vacuum that can increase the efficiency of copper gettering by polysilicon sink up to 5 times, relative to the conventional polysilicon gettering, making it competitive with advanced internal gettering. This field-enhanced gettering method also enables the detection of the trace amount of copper impurities in silicon wafer bulk by the Dynamic Secondary Ion Mass Spectroscopy (DSIMS), by increasing their concentration levels in the polysilicon film well above the detection limit of $3 \times 10^{15}$ copper atom/cm$^3$. This simple method for reduction and measurement of copper contamination in the wafer bulk can also be extended to other transition metals with either positive or negative charge ions in silicon.
Figure 3.2.1. The experimental setup to demonstrate the Cu gettering technique using electric-field-enhanced isothermal annealing.

Figure 3.2.2. Cu depth profile of p+si wafers, with & without negative biased at 11kV/cm after annealed at 760ºC 2 h. Cu gettering efficiency increases significantly with negative bias.