Device Modeling Talk - Corner Mismatch Model

Speaker: Dr. Philip Tan Beow Yew, Silterra Malaysia Sdn. Bhd
Date: 30th November 2018 (Friday)
Time: 2:30pm to 3:30pm
Venue: Nano Lab 2, FOE ground floor
(Open to ALL students and staff)

This talk will discuss the recent works that we have done in Device Modeling - Corner Mismatch Model. We have recently published this work in ICSE 2018 conference in Kuala Lumpur. Mismatch model is a vital importance for analog circuit design especially when the matched device pair is used, for example, the current mirror. Currently, mismatch models only available in the Monte Carlo simulation, where long simulation time is the common problem faced by the analog circuit designers. This problem is resolved by the introduction of the corner mismatch model where the model can be run without Monte Carlo simulation.

Corner mismatch model is an enhancement to the existing Monte Carlo mismatch model. Besides the capability to predict mismatch behavior using Monte Carlo simulation, designers can use the additional model feature to run the fast non-Monte Carlo corner simulation to get the min and max of the mismatch. Other than the fast non-Monte Carlo simulation, the corner mismatch model also allows the designers to specify the amount of mismatch (differences between two matched devices) and which one of the devices in the matched pair has higher or lower Vt (threshold voltage) or Idsat (drain saturation current).

Speaker Biodata

Dr. Philip Tan Beow Yew received Bachelor of Science (Honours), B.Sc.(Hons) degree in Physics and Master of Science, M.Sc. degree in Analog/Digital IC Design from University Putra Malaysia, UPM in 1999 and 2000 respectively, and Doctor of Philosophy, Ph.D. degree in CMOS Transistor Device Characterization and Modeling from University Science Malaysia, USM in 2008.

He has started to work in Silterra Malaysia Sdn. Bhd. foundry in 2000. He was promoted to Senior Manager of Device Modeling in 2016. He has 18 years of hands-on working experience in extracting SPICE models for deep submicron CMOS transistors. He has introduced physical equation in the SPICE model to capture the Hook Shaped Idsat behavior due to STI stress in channel width direction when he was an engineer. He has led his group (LogicHV) to excel in model extraction by introducing new Binning-Hybrid-Macro extraction methodology that combines the advantages from Global models, Binning models, Hybrid models and Sub-Circuit models. He has initiated the development of in-house Device Modeling software tools to automate device modeling works. This enables his group to generate device modeling test chip layout, perform IV and CV measurements and extract SPICE models using in-house developed software tools. He is the instructor for Integrated Circuit Overview class for Silterra's new hires.

Before involving in SPICE modeling works, he has spent a year On-Job-Training as a Process Integration Engineer at LSI Logic Corporation in Oregon, USA. He has given SPICE Modeling tutorial classes in 2007 IEEE Regional Symposium on Microelectronic (RSM) and 2017 IEEE PrimeAsia conferences. He has published 34 international and national IEEE conference papers. He was invited as the reviewer for IEEE Electron Device Letters and IEEE Transactions on Electron Devices journals in 2007 and 2008. He was elevated to IEEE Senior Member (Electron Device Society) in 2009. He was invited as the Keynote Speaker for the 2017 IEEE PrimeAsia conference.